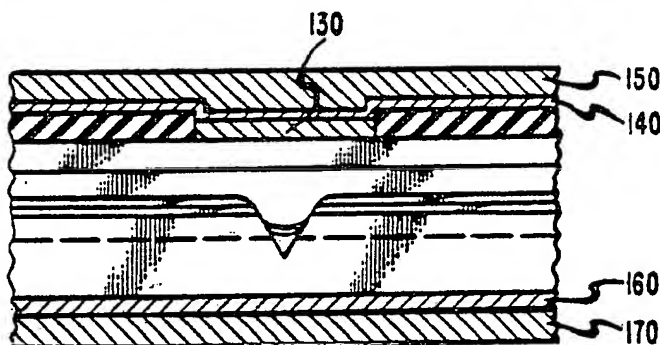




INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification ⁴ : H01L 21/285, 29/40, 33/00	A1	(11) International Publication Number: WO 88/ 00392 (43) International Publication Date: 14 January 1988 (14.01.88)
<p>(21) International Application Number: PCT/US87/01520</p> <p>(22) International Filing Date: 22 June 1987 (22.06.87)</p> <p>(31) Priority Application Number: 878,077</p> <p>(32) Priority Date: 24 June 1986 (24.06.86)</p> <p>(33) Priority Country: US</p> <p>(71) Applicant: AMERICAN TELEPHONE & TELEGRAPH COMPANY [US/US]; 550 Madison Avenue, New York, NY 10022 (US).</p> <p>(72) Inventors: APPELBAUM, Amiram ; 11 Glenwood Road, Fanwood, NJ 07023 (US). ROBBINS, Murray ; 110 Kent Drive, Berkeley Heights, NJ 07922 (US).</p> <p>(74) Agents: HIRSCH, A., E., Jr. et al.; Post Office Box 679, Holmdel, NJ 07733 (US).</p>	<p>(81) Designated States: AT (European patent), BE (European patent), CH (European patent), DE (European patent), FR (European patent), GB (European patent), IT (European patent), JP, LU (European patent), NL (European patent), SE (European patent).</p> <p>Published <i>With international search report. Before the expiration of the time limit for amending the claims and to be republished in the event of the receipt of amendments.</i></p>	

(54) Title: METHOD FOR FABRICATING DEVICES IN III-V SEMICONDUCTOR SUBSTRATES AND DEVICES FORMED THEREBY



(57) Abstract

New technique for forming non-rectifying electrical contacts to III-V semiconductor materials, without the use of dopants or of an alloying procedure. In accordance with this technique, an electrical contact is formed simply by depositing a region of material e.g., 130, (onto the semiconductor material) having a composition which includes at least one metal element and at least one of three specific Group V elements, i.e., P, As, or Sb, and having a bulk electrical resistivity equal to or less than about 250 $\mu\Omega$ -cm. Alternatively, a contact is formed by depositing nickel, or a nickel-containing material essentially free of gold and silver, and having a composition which does not include any of the three Group V elements. The nickel, or nickel-containing material, is then reacted with the substrate to form a region, e.g., 130, including a compound having a composition which includes nickel as well as one of the three Group V elements.

FOR THE PURPOSES OF INFORMATION ONLY

Codes used to identify States party to the PCT on the front pages of pamphlets publishing international applications under the PCT.

AT	Austria	FR	France	ML	Mali
AU	Australia	GA	Gabon	MR	Mauritania
BB	Barbados	GB	United Kingdom	MW	Malawi
BE	Belgium	HU	Hungary	NL	Netherlands
BG	Bulgaria	IT	Italy	NO	Norway
BJ	Benin	JP	Japan	RO	Romania
BR	Brazil	KP	Democratic People's Republic of Korea	SD	Sudan
CF	Central African Republic	KR	Republic of Korea	SE	Sweden
CG	Congo	LI	Liechtenstein	SN	Senegal
CH	Switzerland	LK	Sri Lanka	SU	Soviet Union
CM	Cameroon	LU	Luxembourg	TD	Chad
DE	Germany, Federal Republic of	MC	Monaco	TG	Togo
DK	Denmark	MG	Madagascar	US	United States of America
FI	Finland				

METHOD FOR FABRICATING DEVICES IN III-V
SEMICONDUCTOR SUBSTRATES AND
DEVICES FORMED THEREBY

Background of the Invention

5 1. Field of the Invention

The invention pertains generally to a method for fabricating devices in III-V semiconductor substrates, as well as the resulting devices.

 2. Art Background

A wide variety of devices, including discrete electronic devices, discrete
10 opto-electronic devices (devices which produce an optical output in response to
an electrical input, or vice versa), as well as integrated circuit and integrated
optical devices, are now being fabricated, or have been proposed for fabrication,
in substrates which include III-V semiconductor materials, because these
materials exhibit a number of significant advantages. (A III-V semiconductor
15 material, for purposes of this disclosure, is a semiconductor which includes
Group III and Group V elements.) Included among these advantages is the fact
that the mobility of electrons in the III-V semiconductor materials is much
higher than in other semiconductor materials, such as silicon. As a consequence,
electronic and opto-electronic devices, e.g., discrete transistors, lasers and
20 integrated circuit devices, fabricated in the III-V semiconductor materials are
capable of achieving much higher operating speeds than are the corresponding
devices fabricated in, for example, silicon. In addition, the III-V semiconductor
materials are direct bandgap materials, rather than indirect bandgap materials,
as is the case with silicon. As is known, stimulated emission of light is only
25 achievable in the former type of materials. Consequently, opto-electronic
devices which depend, for their operation, on stimulated light emission, e.g.,
lasers, must be fabricated in direct bandgap materials. Moreover, direct
bandgap materials exhibit much higher quantum efficiencies than indirect
bandgap materials, and therefore the former materials are preferred for the
30 fabrication of optical detector, opto-electronic devices, such as avalanche
photodiode (APD) detectors.

The various types of devices fabricated in III-V semiconductor substrates include a variety of device components, such as active regions (a region of semiconductor material in a light-emitting opto-electronic device from which most of the light is emitted), sources, drains, p-n junctions and heterojunctions.

5 (The term heterojunction, as used in this disclosure, denotes the interface between two semiconductor materials having different compositions or different doping levels.) Each such device also includes one or more metallic wires or metallic runners, generally fabricated from gold (Au), terminating in one or more non-rectifying, low specific contact resistance (LSCR) electrical contacts to

10 the substrate, through which electrical signals are communicated to the device. (As used herein, the term non-rectifying, LSCR electrical contact denotes an electrical contact which permits electrical current flow in two opposed directions across the contact, and exhibits a specific contact resistance less than or equal to about 10^{-4} ohm-cm² in both directions. Significantly, such contacts to III-V

15 semiconductor substrates are essential because the gold (per se) in the gold wires and gold runners yields a rectifying, rather than non-rectifying, electrical contact to III-V semiconductor materials.)

A non-rectifying, LSCR electrical contact to a III-V semiconductor substrate is conventionally formed by depositing, e.g., e-beam evaporating, a

20 region of material which includes gold and a p-type (e.g., zinc or beryllium) or n-type (e.g., tin or germanium) dopant (depending upon whether the underlying semiconductor material is of p-type or n-type conductivity) onto the substrate. Because ultra-high-vacuum conditions are typically not employed, a native oxide (or oxides) of the semiconductor material tends to form on the surface of the

25 substrate during the deposition procedure. Such native oxides are generally undesirable because their presence serves to increase specific contact resistance. Although the surface of the substrate is typically cleaned to remove these oxides, it is generally acknowledged that complete removal of the oxides is impossible. However, the presence of these oxides does not, in this instance,

30 preclude the formation of a LSCR electrical contact. That is, after deposition, the gold-and-dopant-containing region is alloyed at temperatures as high as about 450 degrees Centigrade (C) for periods of time equal to about 7 minutes. Significantly, it is believed that this alloying procedure serves to drive the dopant through the native oxide (or oxides) and into the substrate, and

electrically activate the dopant, to produce an electrical contact having a low specific contact resistance.

While the above alloying procedure does produce useful, non-rectifying, LSCR electrical contacts, this procedure does have a number of disadvantages, including undesirable interactions between the gold and the semiconductor substrate. For example, the relatively high temperatures involved in the alloying process result in the gold diffusing into the substrate, causing decomposition of the substrate material. As a consequence, and if, for example, the substrate material includes indium phosphide (InP), then the resulting free In and P (freed by the decomposition of the InP) tend to diffuse to the surface of the electrical contact, where they may undergo oxidation to form electrically insulating layers. In addition, the relatively high alloying temperatures also result in upward diffusion of the p- or n-type dopant to the surface of the electrical contact, where the dopant also tends to become oxidized to form an electrically insulating layer. Unless great care is taken to remove these insulating layers, the electrical contact will exhibit undesirably high series resistance.

The downward diffusion of gold into the substrate is also undesirable because the presence of gold in, for example, an active region constitutes a non-radiative recombination center, which serves to reduce the useful lifetime of light-emitting opto-electronic devices, such as lasers. In addition, the downward diffusion of gold into a substrate containing a relatively shallow p-n junction (a p-n junction having a depth equal to or less than about one-half micrometer) is undesirable because the gold penetrates through, and thus short circuits, these relatively shallow p-n junctions.

The relatively high alloying temperatures employed in forming the gold electrical contacts are further disadvantageous because they sometimes lead to significant, differential thermal expansions of the materials covering the substrate, which in turn leads to high stress in the substrate. Such high stress is undesirable because it leads to bending of the substrate, which makes conventional lithographic processing very difficult, if not impossible. This high stress often also leads to cracking and/or peeling of material layers overlying the substrate.

The above contact-fabrication procedure is further disadvantageous because it requires that the relative amounts of gold and dopant be precisely controlled to achieve the eutectic composition. Otherwise, the gold may not melt during the alloying process and/or the alloying process may not produce a sufficient or desired interaction between the dopant and the substrate, leading to an undesirably high specific contact resistance.

The above-described problems, resulting from the undesirable interactions between gold and III-V semiconductors, as well as scientific curiosity, have led to investigations of the interactions between various metals, including nickel, and III-V semiconductor substrates, such as InP. (Regarding these investigations see E. Hokelek et al., "A Study of Schottky Contacts on Indium Phosphide", Journal of Applied Physics, Vol. 54, No. 9, September 1983, pp. 5199-5205 and G. J. Hughes et al., "Nickel and Copper on Cleaved Indium Phosphide: Structure, Metallurgy and Electronic Properties," Journal of Physics C: Solid State Physics, Vol.16 (1983); pp. 2391-2405.) In these investigations, the various metals were deposited onto indium phosphide substrates cleaved under ultra-high-vacuum conditions to avoid adsorption of contaminants, such as carbon and oxygen (which might increase specific contact resistance, or preclude the formation of non-rectifying contacts). As a result of these investigations, it was concluded, among other things, that nickel produces a Schottky barrier contact (a rectifying, metal-semiconductor contact) to InP and, moreover, that a relatively thin nickel phosphide layer is formed at the interface between the nickel and the InP. While no connection was made (in these investigations) between the existence of the nickel phosphide layer and the existence of the Schottky barrier contact, it has long been believed that a non-rectifying, LSCR contact between a metal, such as nickel, and a substrate of InP can only be achieved if the metal-InP interface is rich in indium. But the interfacial nickel phosphide layer found in the investigations was, presumably, the result of nickel reacting, i.e. combining, with the phosphorus in the InP substrate. Such a reaction would necessarily produce free indium (In), which (under the resulting In concentration gradient) would diffuse to the surface of the nickel, resulting in a nickel-InP interface which is depleted of In. Significantly, a substantial amount of In was found (presumably the result of upward diffusion) on the surface of the nickel, in these investigations.

Consequently, and on the basis of current beliefs, an In-depleted interface, produced by the formation of an interfacial, nickel phosphide layer, would preclude the formation of a non-rectifying, LSCR contact, and would be consistent with the Schottky barrier contacts found in the investigations.

- 5 Thus, those engaged in the development of III-V semiconductor devices have sought, and continue to seek, new materials and new methods for forming non-rectifying, LSCR electrical contacts to III-V semiconductor substrates.

Summary of the Invention

- 10 The invention embodies a method of fabricating a device in a body which includes Group III - Group V semiconductor material and involves the finding that simply depositing any one of a specific class of compounds onto a p- or n-type III-V semiconductor substrate, having a doping level equal to or greater than about 10^{17} per cubic centimeter (cm^{-3}), yields a non-rectifying, LSCR electrical contact to the substrate. The members of this class of compounds are
- 15 those having compositions which include at least one metal element and at least one of three specific Group V elements, i.e., phosphorus (P), arsenic (As) or antimony (Sb), and having bulk electrical resistivities equal to or less than about 250 micro-ohm-centimeters ($\mu\Omega\text{-cm}$), and preferably equal to or less than about 100 $\mu\Omega\text{-cm}$. In addition, the invention involves the finding that
- 20 depositing nickel, or a nickel-containing material which is essentially free of gold and silver and does not include any of the above three Group V elements, onto a III-V semiconductor material, and then reacting the nickel, or nickel-containing material with the semiconductor material to produce a compound having a composition which includes nickel as well as at least one of the three
- 25 Group V elements, also yields a non-rectifying, LSCR electrical contact. Significantly, these contacts are formed without the use of dopants and without the need for an alloying procedure. Moreover, these contacts are formed (through deposition or deposition followed by chemical reaction) without the use of ultra-high-vacuum conditions, and despite the (presumed) adsorption of
- 30 contaminants and formation of native oxides of the semiconductor material.

By way of example, a non-rectifying, LSCR electrical contact to a semiconductor substrate of, for example, InP is readily formed simply by depositing a region of nickel phosphide directly onto the substrate. Alternatively, a region of nickel is deposited onto the substrate and allowed to

spontaneously react with substrate material to form a relatively thin, interfacial layer of nickel phosphide. Contrary to the conventional wisdom, the (presumably) In-depleted interface between the deposited nickel and the semiconductor substrate does not preclude formation of a non-rectifying, LSCR electrical contact.

After being formed, the inventive LSCR electrical contacts are often subjected to relatively high temperatures during various device fabrication steps. Depending upon the particular compositions of the materials employed in the electrical contacts, these materials may (under the influence of the relatively high temperatures) undergo reactions with the substrate material. As a consequence, Group III and/or Group V elements in the substrate may be freed to diffuse to the surface of the electrical contacts, where they may undergo oxidation to form electrically insulating layers.

To avoid the possibility of reactions during high temperature processing, the compositions of the materials employed in the inventive LSCR electrical contacts are preferably chosen (in accordance with a two-step procedure, described below) to have heats of formation which preclude such reactions.

Significantly, it has been found that non-rectifying, LSCR electrical contacts having compositions which preclude reactions with the III-V semiconductor substrates, which are amorphous, and have thicknesses equal to or greater than about 20 nm, are effective barriers to the diffusion of gold (from overlying gold regions, used to facilitate bonding of gold wires or runners) into underlying substrates. As a consequence, light-emitting opto-electronic devices which include such contacts have significantly increased lifetimes. Moreover, LSCR electrical contacts to relatively shallow p-n junctions are now readily formed, without short-circuiting the p-n junctions.

Brief Description of the Drawings

The invention is described with reference to FIGS. 1-6, which depict the steps involved in fabricating a channel-substrate-buried-heterostructure indium phosphide laser, using the inventive device fabrication method.

Detailed Description

The invention involves a method for fabricating devices in III-V semiconductor substrates, which is distinguished from previous such methods in that it includes a new technique for forming non-rectifying, LSCR electrical

contacts to these substrates. The invention also involves the devices, e.g., transistors, lasers, light-emitting diodes, photodetectors, integrated circuits and integrated optical devices, resulting from the inventive method.

As discussed, the invention involves the finding that non-rectifying, LSCR electrical contacts to p- or n-type III-V semiconductor substrates, having doping levels equal to or greater than about 10^{17} cm^{-3} , are readily formed, using either of two techniques. In the first technique, an electrical contact is formed by first cleaning the substrate (using conventional degreasers and oxide strippers), and then simply depositing, e.g., DC magnetron sputtering, any one of a specific class of compounds onto the substrate. The members of this class of compounds are those having compositions which include at least one metal element and at least one of three specific Group V elements, i.e., P, As or Sb, and having bulk resistivities equal to or less than about $250 \mu\Omega\text{-cm}$, and preferably equal to or less than about $100 \mu\Omega\text{-cm}$. The compounds which meet these requirements are typically (although not exclusively) binary, ternary, or quaternary metallic compounds which include, for example, Ni_3P , Ni_2P , NiP , $\text{Ni}_{11}\text{In}_4\text{P}_2$, Ni_3As , Ni_2As , NiAs , Ni_3Sb , Ni_2Sb , and NiSb .

Significantly, the compound deposition, referred to above, need not take place under ultra-high-vacuum conditions, and, if possible, even ordinary room atmospheric conditions are useful. Surprisingly, and even though contaminants are presumably adsorbed, and native oxides of the semiconductor material are presumed to form, during the time interval between cleaning and deposition, the resulting electrical contact is highly useful, i.e., exhibits a specific contact resistance equal to or less than about 10^{-4} ohm-cm^2 to current flow in two opposed directions.

In the second technique, a non-rectifying, LSCR electrical contact to a III-V semiconductor substrate is formed by (cleaning the substrate and) depositing nickel, or a nickel-containing material which is essentially free of gold and silver and does not include any of the three Group V elements, onto the substrate. Then the deposited material is either induced to react (e.g., heat is supplied), or allowed to spontaneously react (i.e., no external stimulus, such as heat, is supplied), with the substrate to form a compound having a composition which includes both nickel as well as one (or more) of the three Group V elements. (Generally, it cannot be predicted whether any particular set of

deposition conditions will result in a spontaneous reaction between the deposited material and the substrate material to produce the desired compound. However, the presence or absence of the desired compound is readily detected using conventional techniques such as Auger electron spectroscopy. Thus, the utility of a particular deposition procedure for achieving the desired spontaneous reaction is readily determined empirically.)

By way of example, an electrical contact to a substrate of InP is formed by depositing, e.g., e-beam evaporating, a region of nickel directly onto the substrate, and then allowing the nickel to spontaneously react with the substrate (during and after the deposition procedure) to form a relatively thin, interfacial layer of nickel phosphide. (The thickness of this interfacial layer is typically several fractions of a nanometer.) If a thicker layer of nickel phosphide is desired, then the nickel-bearing InP-substrate should, for example, be heated, to react additional nickel with the substrate material. In this regard, it has been found that a relatively thick layer of essentially pure Ni_2P is readily formed by carrying out the heating process (at a temperature of, for example, 300 degrees C) in an atmosphere of forming gas, i.e., an atmosphere which includes about 15 percent (by volume) of H_2 and about 85 percent of N_2 .

It is contemplated that the two techniques, described above, yield non-rectifying, LSCR contacts because Group III elements in the substrate form chemical bonds with the Group V elements in the contacts. Moreover, it is believed that electron-transport across the contact-substrate interface is largely due to thermionic emission.

Significantly, the nickel-containing electrical contacts formed by deposition and reaction are typically crystalline in nature. By contrast, the electrical contacts formed by deposition, alone, are either crystalline or amorphous in nature, depending upon deposition conditions. (For purposes of the invention, a material is amorphous if it either has no grains or, if grains are present, their dimensions are equal to or less than about 50 nm.) For example, if an electrical contact of Ni_2P is deposited using conventional DC magnetron sputtering techniques, then a relatively low substrate-support temperature (e.g., -100 degrees Centigrade) and/or a relatively low sputtering voltage (e.g., 280 volts) yields amorphous Ni_2P . On the other hand, a substrate-support maintained at room temperature (23 degrees Centigrade) and/or a relatively

high sputtering voltage (e.g., 300 volts) yields crystalline Ni_2P . This distinction between the natures of the electrical contacts results in different contact properties. That is, crystalline contacts typically exhibit lower bulk resistivities than amorphous contacts, which leads to reduced series resistance. On the other hand, as discussed more fully below, amorphous contacts are better diffusion barriers than crystalline contacts.

The inventive method for fabricating devices often involves relatively high temperature processing subsequent to the fabrication of a non-rectifying LSCR electrical contact (or contacts). Such high temperature processing may result in chemical reactions between the material of the electrical contact and the substrate material. As a consequence, some Group III and/or Group V elements in the substrate may be freed to diffuse to the surface of the electrical contact, where they may be oxidized to form electrically insulating layers. Such layers may lead to relatively high series resistance.

Preferably, to avoid the high temperature reactions, discussed above, the composition of the material employed in the inventive electrical contact is chosen in accordance with a two-step procedure. In the first step, those compositions are identified which include P, As, or Sb (and nickel, if the contact is formed by deposition and reaction), have bulk resistivities less than or equal to about $250 \mu\Omega\text{-cm}$, and have heats of formation per metal atom (kilocalories per metal atom) which are more negative than that of the substrate composition, i.e., in magnitude (absolute value), the heats of formation per metal atom of the potentially useful compositions are larger than that of the substrate composition. (If a composition includes more than one metal element, then the average heat of formation per metal atom is employed.) Compositions which meet this requirement are (by definition) thermodynamically more stable than the substrate composition. However, one or more of these compositions might still react (under the influence of the relatively high temperatures) with substrate material to form an even more stable composition. To avoid this possibility, these particular compositions are identified and weeded out. That is, during the second step, the most stable composition, i.e., the composition having the most negative heat of formation per metal atom, is initially identified. Then, the magnitude (the absolute value) of the difference between the heat of formation per metal atom of each composition (identified in the first

step) and the most stable composition is calculated. If, for any particular composition, this magnitude is less than the magnitude (absolute value) of the heat of formation per metal atom of the semiconductor composition, then (thermodynamically) this particular composition is precluded from reacting with the substrate to form a more stable composition. Alternatively, and regardless of this requirement, if a particular composition has a larger relative amount of the Group V element than the most stable composition, then this composition too is precluded from reacting with the substrate.

By way of example, if the semiconductor substrate is of InP, then the first step (of the two-step procedure) implies that the potentially useful compositions include Ni_6P_5 , Ni_3P_2 , and Ni_2P . Significantly, Ni_6P_5 is the most stable of these compositions. Applying the criterion of the second step implies that all of these compositions are thermodynamically stable, i.e., will not react with InP. Moreover, NiP is also useful (will not react with InP) because it contains a larger relative amount of P than Ni_6P_5 .

Typically, after an electrical contact is formed, a region of gold (and, perhaps, other materials) is deposited onto the contact to facilitate the bonding of gold wires and/or gold runners to the electrical contact. Significantly, it has been found that material regions which are thermodynamically stable, as defined by the above two-step procedure, are amorphous, and have thicknesses equal to or greater than about 20 nanometers are effective barriers to undesirable interdiffusion of gold (from the overlying gold region) and the underlying semiconductor material. (Such interdiffusion is undesirable for the reasons given above, in relation to conventional gold electrical contacts.) Thus, such materials are useful both as diffusion barriers and as non-rectifying, LSCR electrical contacts. In fact, such material regions are highly useful just as diffusion barriers interposed between any of a variety of electrical contacts and, for example, the corresponding, overlying gold regions.

Among other advantages, the inventive technique for forming electrical contacts makes it possible to form a relatively shallow electrical contact to a relatively shallow p-n junction or a relatively shallow heterojunction (a p-n junction or heterojunction having a depth less than or equal to about 1/2 micrometer), without short-circuiting the p-n junction or heterojunction. (For purposes of the invention, the depth of a p-n junction, or of a heterojunction, is

defined with reference to the device surface, or interface between different material regions of the device, on which the electrical contact is formed, or from, or through which, the electrical contact extends. That is, the depth of a p-n junction formed, for example, by producing a p-type region within an n-type substrate, is defined as the length of a perpendicular extending from a least-squares-fit planar approximation to the above reference surface or reference material interface to the lowest point where the dopant concentration in the p-type region is equal to the dopant concentration in the n-type substrate. On the other hand, the depth of a heterojunction formed by different semiconductor materials is defined as the length of a perpendicular extending from the above least-squares-fit planar approximation to the lowest point of the interface between the two materials, as determined using, for example, Auger electron spectroscopy. Further, the depth of a heterojunction formed by semiconductor materials having the same composition but different doping levels is as defined above, except that the perpendicular extends to the lowest point of the interface between the two materials where the doping level is the average of the doping levels in the two materials as determined, for example, by SIMS analysis.) That is, and as discussed above, the alloying procedure involved in forming a conventional gold contact typically results in gold being diffused downwardly into the semiconductor substrate. If the electrical contact is to a substrate region containing a p-n junction or heterojunction having a depth equal to or less than about 1/2 micrometer, then the gold invariably diffuses more than about 1/2 micrometer, i.e., the gold diffuses into, and through, the junction, short-circuiting the junction. By contrast, the inventive technique involves no alloying procedure. Thus, provided the contact material is thermodynamically stable, amorphous, and has a thickness equal to or greater than about 20 nanometers, both gold and contact material are largely precluded from diffusing downwardly into the semiconductor substrate into electrical contact with the p-n junction or heterojunction.

Yet another advantage of the invention is the fact that it permits the useful lifetimes of light-emitting, discrete opto-electronic and integrated optical devices to be significantly increased. That is, by forming the material compositions with thicknesses equal to or greater than about 20 nanometers, the downward diffusion of gold into the active regions of such devices is largely

precluded. As a consequence, the formation of non-radiative recombination centers is largely avoided.

As a pedagogic aid to an even more complete understanding of the invention, the application of the inventive device fabrication method to the formation of a channel-substrate-buried-heterostructure InP laser, is described below.

With reference to FIGS. 1-6, the laser is formed in a substrate which initially includes just a bulk region 10 of, for example, n-type InP, e.g., a wafer of n-type InP. The doping level within the bulk region 10 is, for example, about $8 \times 10^{17} \text{ cm}^{-3}$.

The first step in the fabrication of the laser is to form a blocking layer 30, i.e., a layer which blocks the flow of currents external to the active region (described below) into the bulk region 10, adjacent to the upper surface 20. The blocking layer 30 is formed, for example, by diffusing a p-type dopant, such as cadmium, into the bulk region 10. The doping level within the blocking layer should be equal to or greater than about $4 \times 10^{18} \text{ cm}^{-3}$ to avoid the flow of undesirable leakage currents across the blocking layer and into the bulk region 10. In addition, the thickness of the blocking layer 30 ranges from about $0.5 \mu\text{m}$ to about $1.5 \mu\text{m}$. Thicknesses less than about $0.5 \mu\text{m}$ are undesirable because they too result in undesirable leakage currents across the blocking layer. Thicknesses greater than about $1.5 \mu\text{m}$ are undesirable because they result in lasers which require undesirably large amounts of electrical power to achieve stimulated light emission.

Alternatively, the blocking layer 30 is formed by depositing a layer of semi-insulating InP onto the surface 20, using conventional metal organic chemical vapor deposition techniques. Here, the term semi-insulating means that the deposited semiconductor material has a bulk resistivity equal to or greater than about 10^7 ohm-cm .

After the formation of the blocking layer 30, an etch mask 40 is formed on the upper surface of the blocking layer. This etch mask includes, for example, a layer of silicon dioxide which is deposited onto the blocking layer 30 using conventional plasma deposition techniques. The etch mask is formed by patterning the silicon dioxide layer using, for example, conventional lithographic techniques. The thickness of the silicon dioxide layer ranges from 110 nm to

about 130 nm. Thicknesses less than about 110 nm are undesirable because they result in an undesirably large number of pinholes in the silicon dioxide. On the other hand, thicknesses greater than about 130 nm are undesirable because they make it difficult to achieve the desired sidewall inclination of the

5 V-groove, described below.

With the etch mask 40 in place, a crystallographic, chemical etchant, e.g., 3:1 HCl:H₃PO₄, is applied to the exposed region of the substrate surface to form a V-groove 50. This V-groove 50 serves to channel, and confine, the electrical current to the active region of the laser. The etchant is chosen to expose (111) facets of the crystalline substrate. Moreover, the width of the V-groove ranges from about 3.5 micrometers (μm) to about 4.5 μm . Widths less than about 3.5 μm , or greater than about 4.5 μm , are undesirable because they result in devices which require an undesirably large amount of electrical power to achieve stimulated emission of light.

15 After the etching of the V-groove 50, and after removing (using conventional chemical etchants) the etch mask 40, an n-type InP buffer region 60 is grown in the bottom of the V-groove 50 (as well as on the surface of the blocking layer 30) using conventional liquid phase epitaxy (LPE) techniques. The thickness of the buffer region, as measured from the bottom of the V-groove, typically ranges from about 0.5 μm to about 1 μm . Unlike the sidewalls of the V-groove, the buffer region 60 is largely free of contaminants and defects.

An undoped, active region 70 of III-V semiconductor material is now grown on the buffer region 60 in the V-groove 50 (as well as on the upper surface of the blocking layer 30) using conventional LPE techniques. To ensure that electrical conduction is largely confined to the active region 70, the bandgap of the semiconductor material employed in the active region should be less than that of the semiconductor material employed both in the blocking layer 30 and in the cladding layer (discussed below). One such useful (active region) material is, for example, (undoped) indium gallium arsenide phosphide (InGaAsP). The thickness of the active region ranges from about 0.2 μm to about 0.7 μm . Thicknesses less than about 0.2 μm are undesirable because such thin regions result in undesirably little stimulated light emission from the laser. Thicknesses greater than about 0.7 μm are undesirable because they result in lasers which require an undesirably large amount of electrical power to achieve

stimulated emission of light.

The growth of the active region 70 is followed by the LPE-growth of a cladding layer 80 and of a cap layer 90. The former is, for example, of p-type InP, while the latter is of p-type indium gallium arsenide (InGaAs). The thickness of the cladding layer, and of the cap layer, is typically about 1 μm .

A (patterned) deposition mask 120 is now formed on the upper surface of the cap layer 90. As discussed below, the deposition mask permits the electrical contact to the laser to be formed in vertical alignment with the active region 70. The deposition mask 120 includes a layer 100 of silicon dioxide which is deposited onto the cap layer 90 using, for example, conventional plasma deposition techniques. In addition, the deposition mask includes a layer 110 of, for example, photoresist. The thickness of the silicon dioxide layer is typically about 0.3 μm , while the thickness of the photoresist is typically about 1 μm . In forming the deposition mask, the photoresist is initially patterned, i.e., a region of the photoresist overlying the active region 70 is removed, using conventional exposure and development techniques. The width of this region (and thus the ultimate width of the electrical contact) is typically about 6 μm . The patterned photoresist layer is then used as an etch mask during the etching of the silicon dioxide layer 100, resulting in the removal of a region of the silicon dioxide layer which also overlies the active region 70. Useful silicon dioxide-etchants include, for example, buffered HF.

An electrical contact to the laser is now produced by depositing, e.g., sputtering, an amorphous region 130 of, for example, Ni_3P_5 onto the exposed upper surface of the cap layer 90. Preferably, the thickness of the region 130 is equal to a greater than about 20 nanometers, to avoid the downward diffusion of gold (from a gold region subsequently formed on the region 130).

Preferably, to enhance the adhesion of the region 130 to the cap layer 90, a layer 140 of titanium is deposited onto the upper surface of the region 130 as well as onto the upper surface of the silicon dioxide layer 100. The thickness of the titanium layer is typically about 5 nanometers.

With the completion of the electrical contact, a layer 150 of gold is deposited onto the upper surface of the titanium layer 140, to facilitate the subsequent bonding of a gold wire to the electrical contact. The thickness of the gold layer is typically about 1 μm .

A second electrical contact is, of course, needed to apply voltages to the laser. This second contact is formed on the backside of the substrate by initially thinning the bulk region 10 (typically by about $75\text{ }\mu\text{m}$) using conventional mechanical lapping, and then depositing successive layers 160 and 5 170 of, respectively, Ni_3P_5 and gold, onto the backside, as described above.

The bulk region 10, which is now an integral part of the laser, is typically a portion of a wafer which, at this point, is cleaved (using conventional techniques) to form the end mirror-facets of the laser device. The laser device is separated from the wafer using saw cuts transverse to the mirror-facets.

10 The final steps in the fabrication of the laser typically involve soldering (at temperatures ranging from about 200 degrees C to about 350 degrees C) the laser to a stud which serves both as a heat sink for the device, as well as a device carrier or package. Then, gold wires are bonded to the gold regions 150 and 170 covering the top and bottom of the laser.

15 Example 1

The lower surface of a 1.27 cm (one-half-inch) diameter indium phosphide wafer, of n-type conductivity, and having a doping level of $8 \times 10^{17}\text{ cm}^{-3}$, was cleaned using conventional degreasers and oxide strippers. Using conventional e-beam evaporation techniques, successive layers of gold, germanium, and gold 20 were deposited onto the cleaned lower surface. The thicknesses of these layers were, respectively, 5 nm, 15 nm, and 100 nm.

The upper surface of the wafer was degreased, and a layer of SiO_2 , having a thickness of 500 nm, was plasma deposited onto the upper surface. A layer of photoresist was spin-deposited onto the SiO_2 , and conventionally 25 lithographically patterned to remove circular regions of photoresist having diameters ranging from about $20\text{ }\mu\text{m}$ to about $200\text{ }\mu\text{m}$. Using the patterned photoresist as an etch mask, the silicon dioxide was chemically etched with buffered HF to expose corresponding circular surface areas of the indium phosphide.

30 A layer of Ni_2P , having a thickness of about 100 nm, was deposited onto the exposed, circular surface areas of the wafer, as well as onto the photoresist, using DC magnetron sputtering. The gas within the sputtering chamber was argon, the pressure of the gas was 1.6 Pa (12 millitorr), and the DC voltage was 300 volts. The Ni_2P -covered photoresist was then stripped from the wafer using

conventional chemical etchants.

The conventional Cox and Strack technique (see R. H. Cox and H. Strack, Solid State Electronics, Vol. 10, page 1213 (1967)) was employed to measure the specific contact resistance at each of the Ni_2P -covered regions of the wafer, using electrical currents of opposite polarity. In all cases, the specific contact resistance was equal to or less than about $3 \times 10^{-6} \text{ ohm-cm}^2$.

Example 2

A 1.27 cm (one-half-inch) indium phosphide wafer was processed, as in Example 1, except that a different technique was used to form the circular regions of Ni_2P on the upper surface of the wafer. That is, after the photoresist and SiO_2 were patterned, a 100 nm-thick layer of Ni was e-beam evaporated onto the exposed, circular surface areas of the wafer, as well as onto the photoresist. After stripping the Ni-covered photoresist, the wafer was placed in an atmosphere of forming gas, and heated to a temperature of 300 degrees C for 30 minutes to produce circular regions of Ni_2P , having thicknesses of about 130 nm, on the wafer.

Using the technique employed in Example 1, the specific contact resistance, in all cases, was found to be equal to or less than about $3 \times 10^{-6} \text{ ohm-cm}^2$.

Claims

1. A method for fabricating a device in a body which includes III-V semiconductor material, comprising the steps of:
forming a non-rectifying, low-specific-contact-resistance electrical contact
5 to a region of said body having a doping level equal to or greater than about 10^{17} cm^{-3} ; and
completing the fabrication of said device,
CHARACTERIZED IN THAT
said forming step includes the step of
10 (a) depositing a metal-containing first region of material onto said region of said body, or
(b) depositing a nickel-containing second region of material, essentially free of gold and silver, onto said region of said body and reacting said second region with said semiconductor material to form a nickel-containing third region
15 of material,
each of said first and third regions having a composition which includes at least one element chosen from the group consisting of phosphorus, arsenic and antimony, and having a bulk resistivity equal to or less than about $250 \mu\Omega\text{-cm}$.
- 20 2. The method according to claim 1
CHARACTERIZED IN THAT
said metal of said first region includes nickel.
3. The method according to claim 1,
CHARACTERIZED IN THAT
25 said composition is chosen to preclude chemical reactions between said first or said third of material and said semiconductor material.
4. The method according to claim 1,
CHARACTERIZED IN THAT
said first region of material, or said third region of material, is
30 amorphous.
5. The method according to claim 1,
CHARACTERIZED IN THAT

said first region of material, or said third region of material, has a thickness equal to or greater than about 20 nanometers.

6. The method according to claim 1,

CHARACTERIZED IN THAT

5 said device includes a discrete electronic device or an integrated circuit device or an opto-electronic or an integrated optical device.

7. The method according to claim 6,

CHARACTERIZED IN THAT

said discrete electronic device includes a transistor.

10 8. The method according to claim 6,

CHARACTERIZED IN THAT

said opto-electronic device includes a laser or a light-emitting diode or a photodetector.

9. A method according to claim 1,

15 CHARACTERIZED IN THAT

said body includes a surface or material interface, and said body region includes a p-n junction or a heterojunction adjacent said surface or material interface;

20 said p-n junction or said heterojunction has a depth, as measured from said surface or material interface, equal to or less than about 1/2 micrometer, a non-rectifying, low-specific-contact-resistance electrical contact is on and/or extends from or through said surface or material interface, and

25 said electrical contact includes material which, if it extends into said body, does not extend into electrical contact with said p-n junction or said heterojunction.

1/2

FIG. 1

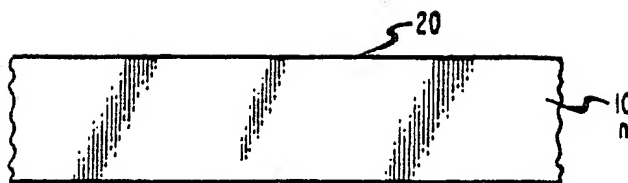


FIG. 2



FIG. 3

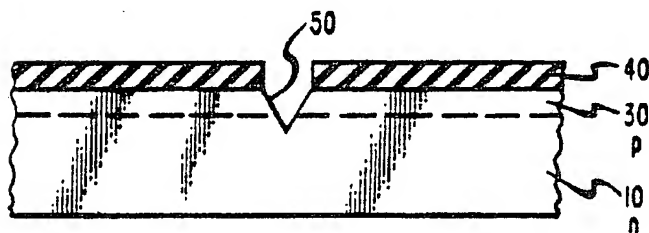


FIG. 4

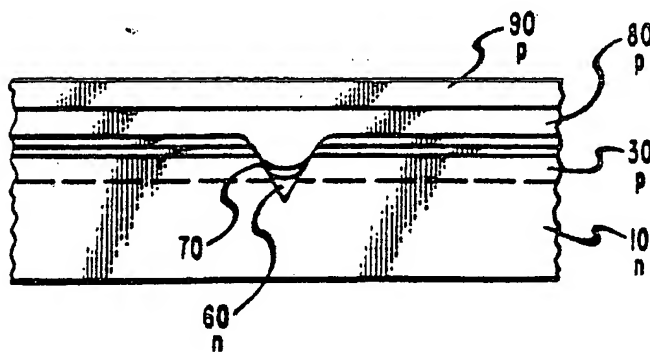


FIG. 5

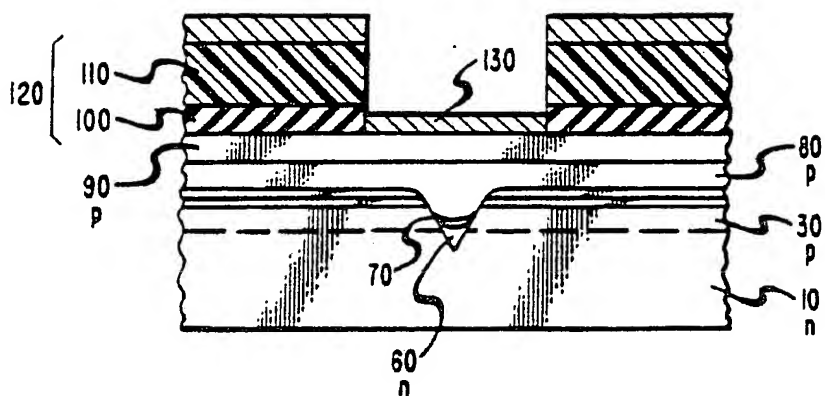
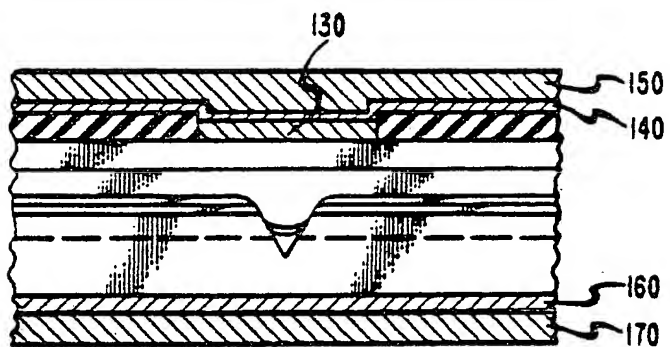


FIG. 6



INTERNATIONAL SEARCH REPORT

International Application No

PCT/US 87/01520

I. CLASSIFICATION OF SUBJECT MATTER (if several classification symbols apply, indicate all) * According to International Patent Classification (IPC) or to both National Classification and IPC IPC ⁴ : H 01 L 21/285; H 01 L 29/40; H 01 L 33/00														
II. FIELDS SEARCHED <div style="text-align: center; border-top: 1px solid black; border-bottom: 1px solid black;">Minimum Documentation Searched ⁷</div> <table style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 25%; border-bottom: 1px solid black;">Classification System</td> <td style="border-bottom: 1px solid black;">Classification Symbols</td> </tr> <tr> <td style="border: 1px solid black; text-align: center;">IPC⁴</td> <td style="border: 1px solid black; text-align: center;">H 01 L</td> </tr> </table> <div style="text-align: center; border-top: 1px solid black; border-bottom: 1px solid black;">Documentation Searched other than Minimum Documentation to the extent that such Documents are Included in the Fields Searched ⁸</div>			Classification System	Classification Symbols	IPC ⁴	H 01 L								
Classification System	Classification Symbols													
IPC ⁴	H 01 L													
III. DOCUMENTS CONSIDERED TO BE RELEVANT ⁹ <table style="width: 100%; border-collapse: collapse;"> <tr> <th style="width: 10%; border-bottom: 1px solid black;">Category *</th> <th style="width: 60%; border-bottom: 1px solid black;">Citation of Document, ¹¹ with indication, where appropriate, of the relevant passages ¹²</th> <th style="width: 30%; border-bottom: 1px solid black;">Relevant to Claim No. ¹³</th> </tr> <tr> <td style="text-align: center; vertical-align: top;">A</td> <td style="vertical-align: top;">Materials Letters, volume 3, no. 7,8, May 1985, Elsevier Science Publishers B.V., (Amsterdam, NL), S.R. Smith et al.: "Stable ohmic contacts to n-GaAs using ion-beam mixing", pages 294-298 see the whole document --</td> <td style="text-align: center; vertical-align: top;">1,2,6,9</td> </tr> <tr> <td style="text-align: center; vertical-align: top;">A</td> <td style="vertical-align: top;">GB, A, 2024506 (WESTERN ELECTRIC CO.) 9 January 1980 see the whole document --</td> <td style="text-align: center; vertical-align: top;">1,6-9</td> </tr> <tr> <td style="text-align: center; vertical-align: top;">A</td> <td style="vertical-align: top;">Journal of Physics C: Solid State Physics, volume 16, 1983, The Institute of Physics, (London; GB), G.J. Hughes et al.: "Nickel and copper on cleaved indium phosphide: structure, metallurgy and electronic properties", pages 2391-2406 see paragraph 1: "Introduction"; paragraph 4: "Discussion" cited in the application --</td> <td style="text-align: center; vertical-align: top;">1-3</td> </tr> </table>			Category *	Citation of Document, ¹¹ with indication, where appropriate, of the relevant passages ¹²	Relevant to Claim No. ¹³	A	Materials Letters, volume 3, no. 7,8, May 1985, Elsevier Science Publishers B.V., (Amsterdam, NL), S.R. Smith et al.: "Stable ohmic contacts to n-GaAs using ion-beam mixing", pages 294-298 see the whole document --	1,2,6,9	A	GB, A, 2024506 (WESTERN ELECTRIC CO.) 9 January 1980 see the whole document --	1,6-9	A	Journal of Physics C: Solid State Physics, volume 16, 1983, The Institute of Physics, (London; GB), G.J. Hughes et al.: "Nickel and copper on cleaved indium phosphide: structure, metallurgy and electronic properties", pages 2391-2406 see paragraph 1: "Introduction"; paragraph 4: "Discussion" cited in the application --	1-3
Category *	Citation of Document, ¹¹ with indication, where appropriate, of the relevant passages ¹²	Relevant to Claim No. ¹³												
A	Materials Letters, volume 3, no. 7,8, May 1985, Elsevier Science Publishers B.V., (Amsterdam, NL), S.R. Smith et al.: "Stable ohmic contacts to n-GaAs using ion-beam mixing", pages 294-298 see the whole document --	1,2,6,9												
A	GB, A, 2024506 (WESTERN ELECTRIC CO.) 9 January 1980 see the whole document --	1,6-9												
A	Journal of Physics C: Solid State Physics, volume 16, 1983, The Institute of Physics, (London; GB), G.J. Hughes et al.: "Nickel and copper on cleaved indium phosphide: structure, metallurgy and electronic properties", pages 2391-2406 see paragraph 1: "Introduction"; paragraph 4: "Discussion" cited in the application --	1-3												
<div style="display: flex; justify-content: space-between;"> <div style="width: 45%;"> <p>* Special categories of cited documents: ¹⁰</p> <p>"A" document defining the general state of the art which is not considered to be of particular relevance</p> <p>"E" earlier document but published on or after the international filing date</p> <p>"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)</p> <p>"O" document referring to an oral disclosure, use, exhibition or other means</p> <p>"P" document published prior to the international filing date but later than the priority date claimed</p> </div> <div style="width: 45%;"> <p>"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention</p> <p>"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step</p> <p>"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.</p> <p>"&" document member of the same patent family</p> </div> </div>														
IV. CERTIFICATION <table style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 50%; border-bottom: 1px solid black;">Date of the Actual Completion of the International Search</td> <td style="width: 50%; border-bottom: 1px solid black;">Date of Mailing of this International Search Report</td> </tr> <tr> <td style="border-bottom: 1px solid black; text-align: center;">21st September 1987</td> <td style="border-bottom: 1px solid black; text-align: center;">118 NOV 1987</td> </tr> <tr> <td style="border-bottom: 1px solid black;">International Searching Authority</td> <td style="border-bottom: 1px solid black;">Signature of Authorized Officer</td> </tr> <tr> <td style="text-align: center;">EUROPEAN PATENT OFFICE</td> <td style="text-align: center;">M. VAN MOL </td> </tr> </table>			Date of the Actual Completion of the International Search	Date of Mailing of this International Search Report	21st September 1987	118 NOV 1987	International Searching Authority	Signature of Authorized Officer	EUROPEAN PATENT OFFICE	M. VAN MOL				
Date of the Actual Completion of the International Search	Date of Mailing of this International Search Report													
21st September 1987	118 NOV 1987													
International Searching Authority	Signature of Authorized Officer													
EUROPEAN PATENT OFFICE	M. VAN MOL													

III. DOCUMENTS CONSIDERED TO BE RELEVANT (CONTINUED FROM THE SECOND SHEET)		
Category*	Citation of Document, with indication, where appropriate, of the relevant passages	Relevant to Claim No
A	Thin Solid Films, volume 70, no. 1, July 1980, Elsevier Sequoia S.A., (Lausanne, CH), M. Ogawa: "Alloying reaction in thin nickel films deposited on GaAs", pages 181-189 see the whole document	1
A	Solid-State Electronics, volume 26, no. 3, March 1983, Pergamon Press Ltd, (Exeter, GB), A. Piotrowska et al.: "Ohmic contacts to III-V compound semiconductors: a review of fabrication techniques", pages 179-197	
A	Journal of Applied Physics, volume 54, no. 9, September 1983, American Institute of Physics, (New York, US), E. Hökelek et al.: "A study of Schottky contacts on indium phosphide", pages 5199-5205 cited in the application	

ANNEX TO THE INTERNATIONAL SEARCH REPORT ON

INTERNATIONAL APPLICATION NO. PCT/US 87/01520 (SA 17750)

This Annex lists the patent family members relating to the patent documents cited in the above-mentioned international search report. The members are as contained in the European Patent Office EDP file on 29/09/87

The European Patent Office is in no way liable for these particulars which are merely given for the purpose of information.

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
GB-A- 2024506	09/01/80	BE-A- 877189	15/10/79
		NL-A- 7904979	02/01/80
		FR-A,B 2430090	25/01/80
		DE-A- 2925791	03/01/80
		US-A- 4186410	29/01/80
		JP-A- 55004999	14/01/80
		CA-A- 1125924	15/06/82